KALRAY

Kalray MPPA MANYCORE ®
A new era of computing for embedded application

Embedded System Symposium

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Presentation Outline

- Kalray company and vision
- The MPPA MANYCORE processor and its architecture
- Software programming models
- Application domains

Kalray at a glance

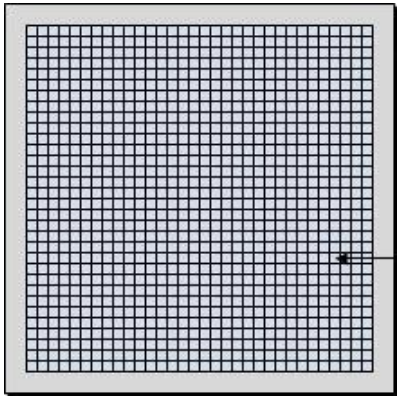
- Founded in 2008 – located in Paris, Grenoble (France), Tokyo (Japan), Sunnyvale (USA)
- Kalray Japan created 2011, headed by Kazumi SUGIYAMA President
- 55+ people (45 in R&D)

- Multi-Purpose Processing Array technology MPPA MANYCORE®
- Independent hardware and software technology
- Portfolio of 64 patents

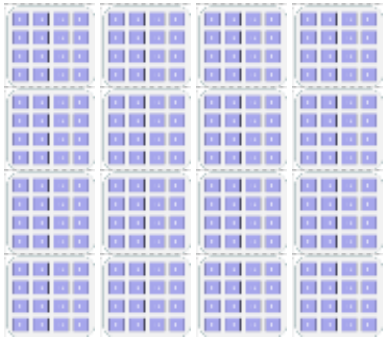
- Targeting the industrial embedded and computing intensive markets

Kalray's Vision

From FPGA / ASIC **TO** MANYCORE processor



FPGA, ASIC, SoC
- Millions gates
- Hard programming



Manycore processor
- **1000s of cores**
- **Soft programming**

The breakthrough *: move from a hardware world made of IP blocks to a generic, scalable computing platform capable based on software components*

First MPPA®-256 Chips with CMOS 28nm TSMC

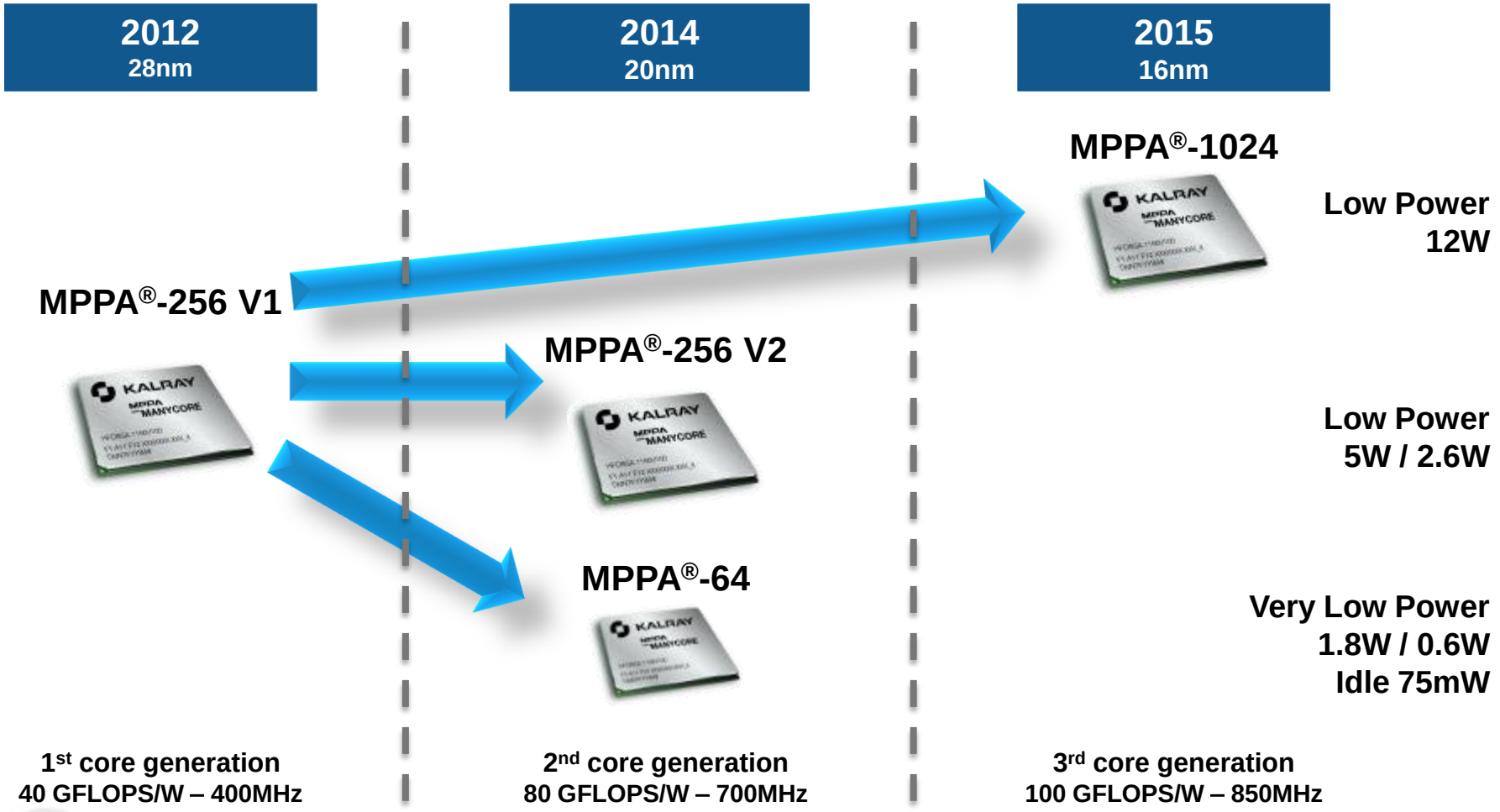
256 Processing Engine cores + 32 Resource Management cores

In production

- High processing performance
  - 700 GOPS – 230 GFLOPS
- High energy Efficiency
  - 5W Typical
  - Advanced power management
- Execution time predictability
- Architecture and software scalability
- Software programmable
  - High level programming models
  - Advanced debugging and tracing

MPPA MANYCORE Roadmap

Architecture scalability for high performances and low power



A Global Product Offer

MPPA MANYCORE

Powerful, Low Power and Programmable Processors

MPPA ACCESSCORE

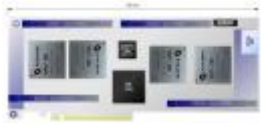
C/C++ based Software Development Kit (SDK) for massively parallel programing

MPPA DEVELOPER

Development platform
Reference Design Board

MPPA BOARDS

Reference Design board
Application specific boards
Multi-MPPA or Single-MPPA boards



Application Domains

INTENSIVE COMPUTING

- Oil and Gas
- Finance
- Numerical Simulation
- Life sciences

IMAGE & VIDEO

- Video Broadcast
- Medical Imaging
- Digital Cinema
- Vision, Video surveillance

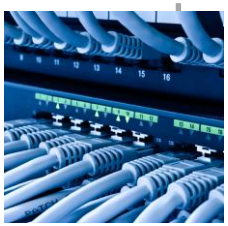
EMBEDDED SYSTEMS

- Transport
- Signal Processing
- Aerospace/Defence
- Industrial Automation

TELECOM

- Network Traffic Analysis
- Security Services
- Software Defined Radio

(Market under investigation)



*Kalray also serves the **Academic market***
(universities and research institutions)

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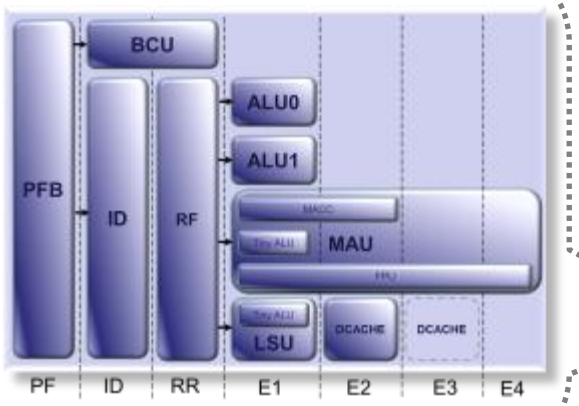
MPPA MANYCORE architecture

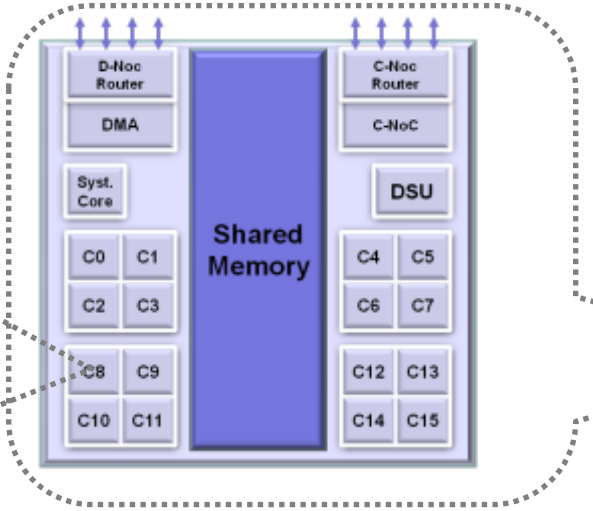
MPPA®-256 Processor Architecture
3 levels of parallelism on a single chip

Instruction Level Parallelism



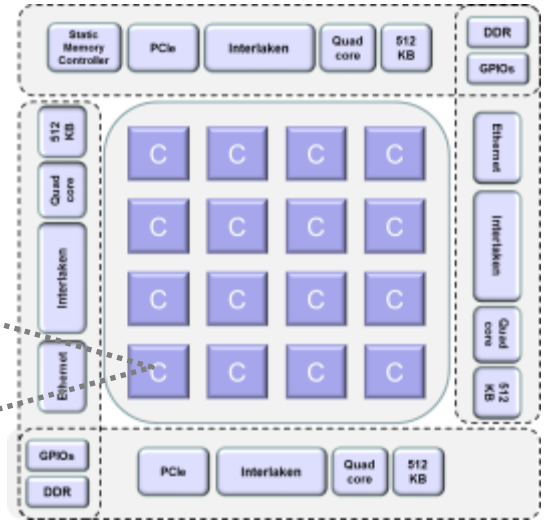
VLIW Core

Thread Level Parallelism



Compute Cluster

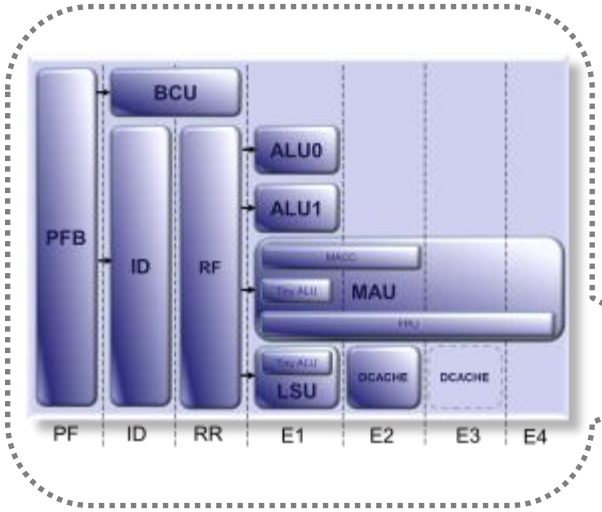
Process Level Parallelism



Manycore Processor

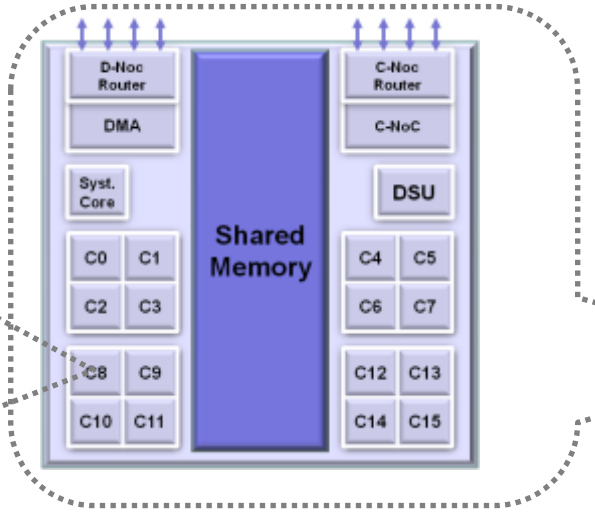
MPPA®-256 Processor Architecture
3 levels of time determinism

Time Compositional Core (repeatable execution times)



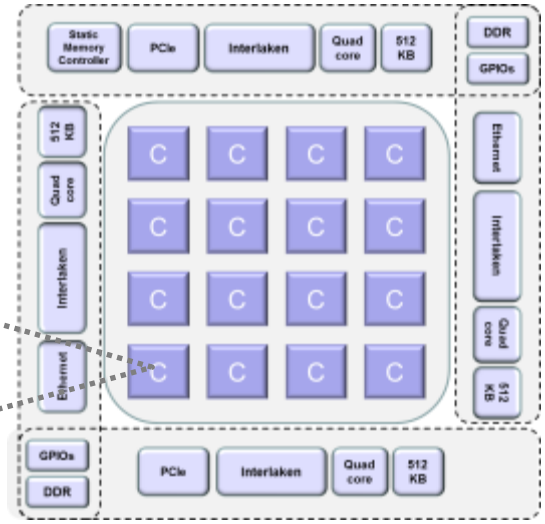
VLIW Core

Flat Memory Hierarchy
Conflict free memory access



Compute Cluster

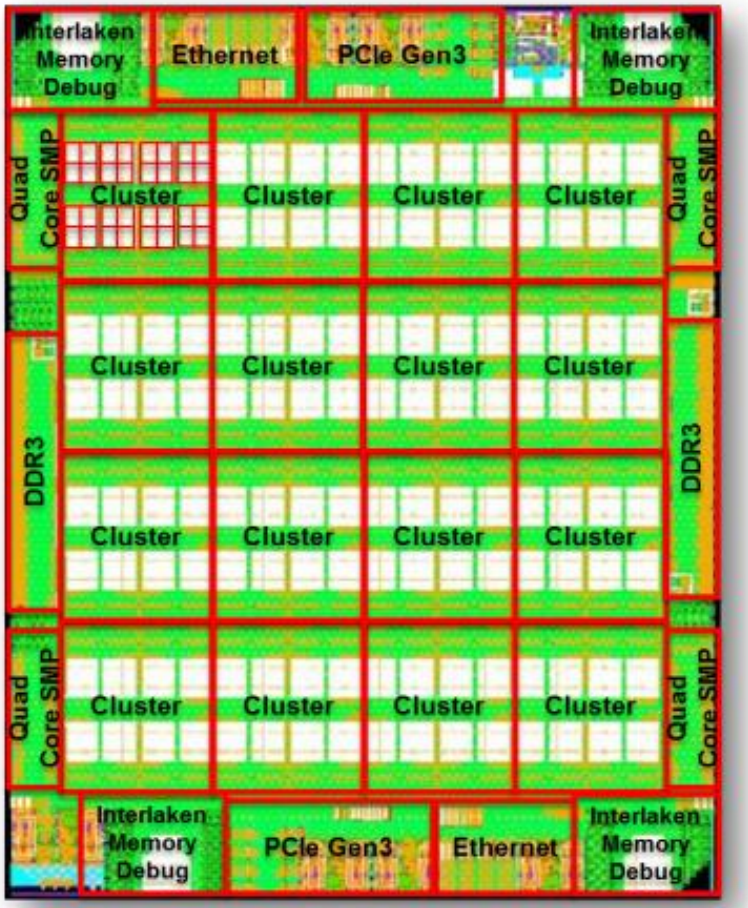
Network-on-chip Quality of Service



Manycore Processor

MPPA has high execution predictability

MPPA®-256 Processor I/O Interfaces



- DDR3 Memory interfaces
- PCIe Gen3 interface
- **1G/10G/40G Ethernet interfaces**
- **SPI/I2C/UART interfaces**
- Universal Static Memory Controller (NAND/NOR/SRAM)
- **GPIOs with Direct NoC Access**
- NoC extension through Interlaken interface (NoC Express)

MPPA ® fits high performance, time constrained embedded applications

- Architectural support
  - K1 VLIW core
    - Amenable to precise static timing analysis
  - Multi-banked memory
    - Conflict-free accesses on address ranges
  - Network-on-chip QoS
    - Guaranteed bandwidth
    - Bounded latency
  - High-speed interfaces
    - Stream data in/out of the MPPA through NoC
- Tools and library support
  - Cyclostatic Dataflow programming language and compiler
  - OpenCL implementation with real-time processing extension (2014)

Software Programming Models

Kalray Software Development Kit

MPPA® ACCESSCORE – MPPA® ACCESSLIB

Linux Today

Microsoft Windows Q4 2013

Standard C/C++ Programming Environment

Simulators, Profilers, Debuggers & System Trace

Operating Systems & Device Drivers

Dataflow Programming
FPGA Style

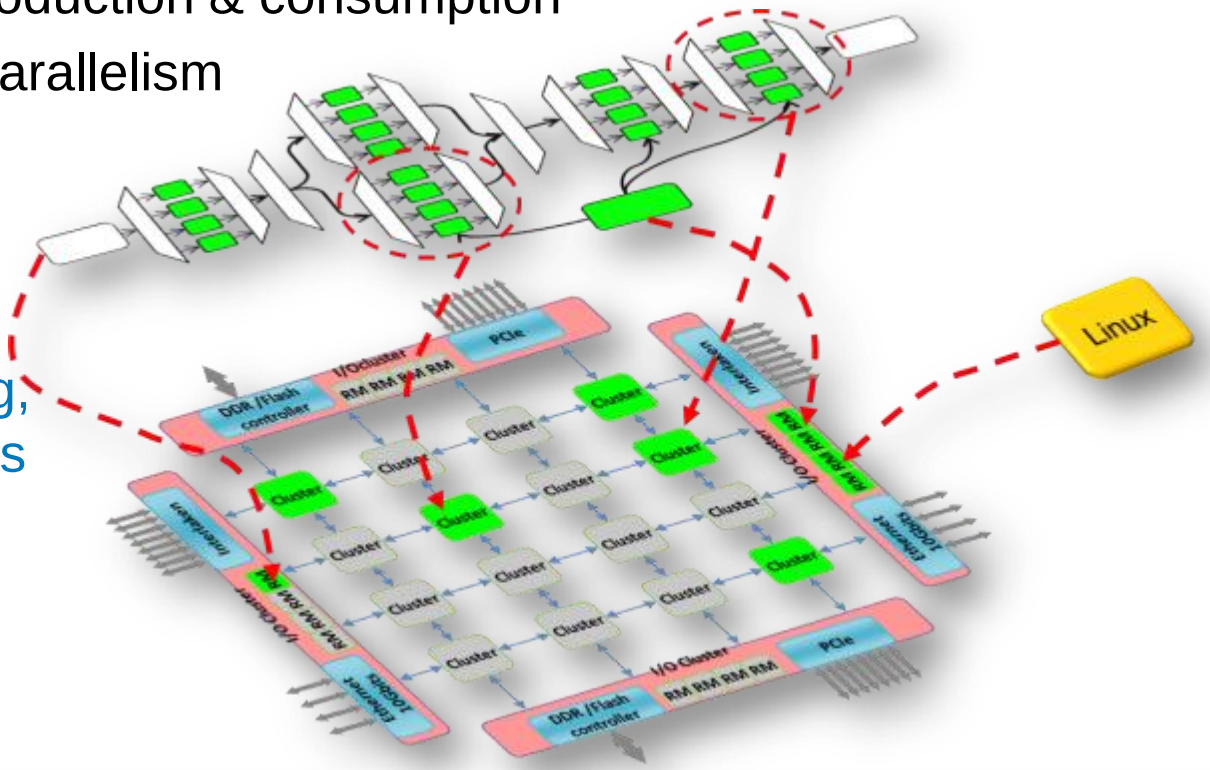
POSIX-Level Programming
DSP Style

Streaming Programming
GPU Style

Dataflow Programming Environment

- Language Sigma-C is a superset of C99
- Computation blocks and communication graph written in C
- Cyclostatic data production & consumption
- Task and/or data parallelism

Automatic mapping on MPPA® memory, computing, & communication resources



Sigma-C Agent Example

agent keyword followed by the name of the agent

interface section for input/ output channels

state machine specification for data production & consumption

exchange keyword flags direct operations on input / output channels

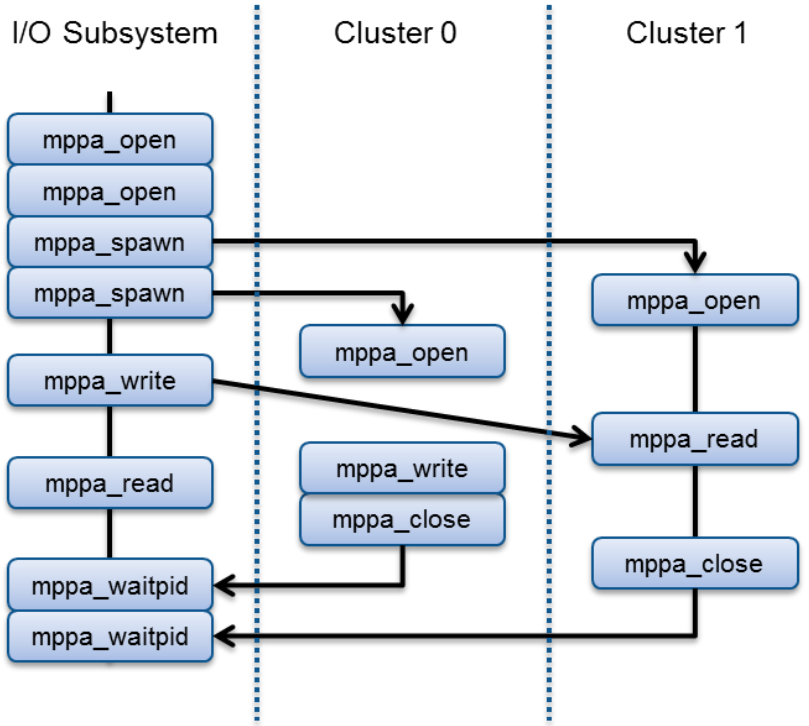
standard C code within the agent

start function is an infinite loop

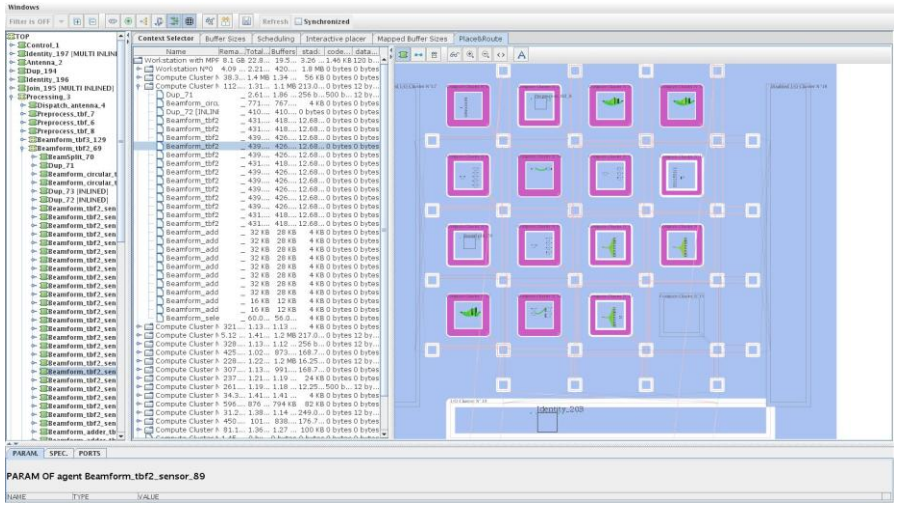
```
agent Inverter()
{
   interface
   {
      in<unsigned char> input; /*< input byte stream */
      out<unsigned char> output; /*< output byte stream */

      spec{input; output};
   }

   void invert (void) exchange (input pel_in, output pel_out)
   {
         pel_out = 255 - pel_in;
   }

   void start ()
   {
         invert();
   }
}
```

POSIX-Level Programming Environment

- POSIX-like process management
  - Spawn 16 processes from the I/O subsystem
  - Process execution on the 16 clusters start with main(argc, argv) and environment
- Inter Process Communication (IPC)
  - POSIX file descriptor operations on 'NoC Connectors'
  - Inspired by supercomputer communication and synchronization primitives
- Multi-threading inside clusters
  - Standard GCC/G++ OpenMP support
    - #pragma for thread-level parallelism
    - Compiler automatically creates threads
  - POSIX threads interface
    - Explicit thread-level parallelism

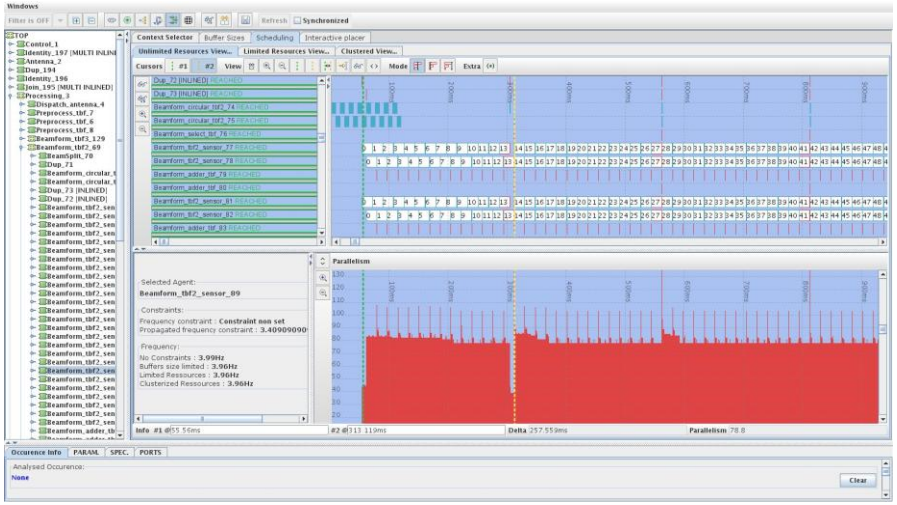


State of the art Debug/Profile/Trace toolsls



< Application Mapping Analysis

Application Performance Analysis >



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Sample Applications

Running Demos at ESS 2013

Feature points (Harris + Sirf)
30 fps / 1080p / 2 clusters

Edge Detection (Sobel Filter)
120fps /1080p / 2 clusters

Line detection (Hough Transform)

Pedestrian detection (Viola-Jones)

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Thank you for your attention
www.kalray.eu

Come meet us at our booth